WHAT IS CLAIMED IS:

1. A latch block comprising:

(a) a plurality of concatenated latch units, each latch unit comprising a latch and a comparator;

(b) a parity bit latch connected to the comparator of a last one of the plurality of concatenated latch units; and

(c) a parity bit comparator in communication with the parity bit latch and with the comparator of the last one of the plurality of latch units.

2. The circuit of claim 1, wherein each latch unit further comprises a fuse connected to the latch within the latch unit.

3. The circuit of claim 2, wherein the comparator is configured to operate in accordance with XOR logic functionality.

4. The circuit of claim 2, wherein each latch comprises a reset node connected to a transistor that is in series with a fuse of the latch.

5. The circuit of claim 2, wherein the parity bit latch stores a parity bit indicating whether an odd or even number of fuses within the latch is blown.

6. The circuit of claim 1, wherein the parity bit comparator flips in the event of a change in the parity bit or the parity bit latch.

7. The circuit of claim 2, wherein the parity bit comparator flips in the event of a change in the parity bit or the parity bit latch.

8. The circuit of claim 6, wherein said plurality of latch units comprise a plurality of N interleaved chains of latch units, such that, after a single strike event, a parity bit flip occurs after any number except a multiple of 2N of simultaneous latch errors within the latch block, said simultaneous latch errors being distributed as a multiple of two latch errors in each of N blocks.

9. The circuit of claim 7 wherein said plurality of successive latch units comprise a plurality of N interleaved chains of latch units, such that, after a single strike event, a parity bit flip occurs after any number except a multiple of 2N of simultaneous latch errors within the latch block, said simultaneous latch errors being distributed as a multiple of two latch errors in each of N blocks.

10. A circuit, comprising :

(a) a latch block including a plurality of successive latch units, each latch unit comprising a latch and a comparator;

(b) a parity bit latch connected to the comparator of a last one of the plurality of concatenated latch units;

(c) a parity bit comparator in communication with the parity bit latch and with the comparator of the last one of the plurality of latch units;

(d) a detector connected to the output of the parity bit comparator; and

(e) a signal-generating device connected to the detector, wherein signals to reset the latch block are produced upon detection of the parity bit flip.

11. The circuit of claim 9, wherein each latch unit further comprises a fuse element connected to the latch within the latch unit.

12. The circuit of claim 9, wherein the plurality of successive latch units comprise a plurality of N interleaved chains of latch units, such that, after a single strike event, a parity bit flip occurs after any number except a multiple of 2N of simultaneous latch errors within the latch block, said multiple of 2N of simultaneous latch errors being distributed as a multiple of two latch errors in each of N blocks.

13. The circuit of claim 10, wherein the plurality of successive latch units comprise a plurality of N interleaved chains of latch units, such that a parity bit flip occurs after any number

except for a multiple of 2N of simultaneous latch errors within the latch block, said multiple of 2N of simultaneous latch errors being distributed as a multiple of two latch errors in each of N blocks.

14. A method for automatically detecting latch soft errors in a latch block, comprising:

(a) arranging a series of latch units, each latch unit comprising a latch and a comparator, such that a comparator of at least one latch unit receives input from a comparator of a preceding latch unit and input from its associated latch;

(b) monitoring an output of a comparator of a final latch unit using a parity bit comparator;

(c) monitoring an output of a latch used to store output of the comparator of the final latch unit using the parity bit comparator; and

(d) detecting a parity bit flip by receiving a change in the output of the parity bit comparator.

15. The method of claim 14, further comprising:

(a) sending a message indicating a parity bit flip to a signal generator;

(b) sending a signal to reset the latches to a default value in response to the message;

(c) resetting of the latch used to store the output of the comparator of the final latch unit; and

(d) rereading all fuses associated with the latch units.

16. The method of claim 14, further comprising:

(a) notifying a signal generator of a latch reset condition;

(b) interrogating the activity in circuitry associated with the fuse block;

(c) receiving an idle status signal from circuitry associated with the fuse block;

(d) sending a signal to reset the latches to a default value;

(e) resetting the latch used to store the output of the comparator of the final latch unit; and

(f) rereading all fuses associated with the latch units.

17. The method of claim 15, wherein the signal generator sends a signal to reset the latches immediately upon receiving a parity bit flip message.